A Wearable Bio-signal Processing System with Ultra-low-power SoC and Collaborative Neural Network Classifier for Low Dimensional Data Communication

Yijie Wei, Qiankai Cao, Levi Hargrove, Jie Gu

Abstract— **In this paper, a real time physiological signal classification system with an integrated ultra-low power collaborative neural network classifier is presented. The developed system includes a specially designed system-on-chip (SoC) and a wireless communication module that transmits classification results to a smartphone app as a convenient user interface in real-time training. The customized SoC provides ultra-low-power and low-latency sensing and classification on physiological signals, e.g. EMG and ECG. A special collaborative neural network classifier was implemented to allow multiple chips to collaborate on classification. As a result, only low dimensional data is being transmitted over the network, significantly reducing data communication across multiple modules. A demonstration of EMG based gesture classification shows 1100X less power consumption from the developed SoC compared with conventional embedded solutions. The transmission of only low dimensional data from the collaborative neural network classifier leads to a 50X reduction of data communication and associated energy for multiple sensing cites.**

I. Introduction

Nourished by the rapid development of wearable electronic devices, the new generation of human assistive biomedical devices with built-in computational intelligence has brought tremendous benefits and improvements to the quality of our life. While smartphones have been most commonly used as personal assistive devices, they lack the measurement support of specific physiological signals, e.g. electromyography (EMG), Electrocardiography (ECG), and low-latency real-time computing capabilities. As a result, more advanced health-care systems utilize various sensor technology, or sensor fusion techniques, to provide deeper diagnosis and more accurate detection of human activities. The commonly used sensing schemes for such a wearable biomedical system include sensors for EMG, ECG, Electroencephalogram (EEG), accelerometers, inertial sensors, electrodermal sensors, strain/torque sensors, etc. Utilizing embedded classifiers, this kind of health-care biomedical system supports low-latency real-time physiological data processing aimed to classify human's activities, e.g. gesture recognition, fall detection or critical medical states, e.g. seizure capturing. Recent examples of such biomedical system include EMG based detection system for prosthetic arms [1-2], EMG based speech recognition system [3], inertia sensor-based motion capture suit for virtual reality technology [4], accelerometer-based fall detection device for Parkinson's disease [5, 6], EMG and ECG detection devices for sleep therapy [7, 8], and Electrodermal conductance sensor-based human emotion/stress detection system [9].

With the recent advancement of artificial intelligence, the classification of bio-signals, e.g. EMG, ECG, EEG, using advanced machine learning techniques has become an essential requirement while also introduces huge computing challenges to wearable biomedical devices. For instance, for a system of robotic prosthetic arms, a large number of channels, e.g. 46 to 72 channels are being processed in real-time with very low latency requirements leading to tremendous burdens on computing devices [10].

For such a real-time bio-signal processing system, four major metrics define the system performance, i.e. classification accuracy, computing latency, data communication efficiency and power consumption. For achieving higher accuracy, researchers have proposed a variety of bio-signal processing algorithms based on different machine learning algorithms including decision trees [11], support vector machine (SVM) classifiers [12], principal component analysis (PCA) [13], convolutional neural networks (CNN) [14, 15]. For instance, it was reported that the accuracy of the decision tree could achieve 88.1% in seizure classify while still providing high efficiency in energy, area and latency [11]. An SVM based system-on-chip (SoC) achieved an accuracy of up to 95% for seizure detection [12]. A PCA-driven detection of heart rate was proposed to provide contactless monitoring through video data [13]. Furthermore, a CNN based model was proposed in recognition of epileptic seizures by converting the EEG signal into spectrogram stacks [14]. To achieve low power consumption, an analog front end (AFE) circuit has been developed with a power consumption of only 1.4μW for a wearable ECG monitoring system [16]. An event-driven Analog-to-Digital Converter (ADC) for wireless ECG sensors was developed for reducing sampling points by 25% for ECG signals compared with the conventional Nyquist sampling scheme [17].

Despite a large amount of implementation presented so far in bio-signal processing, most of the existing demonstrations suffer from the following issues: (1) either numerous chips need to be used for sensing, amplification, and digital classification or a large amount of raw data has to be

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Yijie Wei, Qiankai Cao, Jie Gu are with Northwestern University, Evanston, IL 60201 USA (e-mail: yijiewei2019@u.northwestern.edu, qiankaicao2019@ u.northwestern.edu, jgu@northwestern.edu).

Levi Hargrove is with the Sherly Ryan Ability Lab, Chicago, IL 60611 USA (e-mail: l-hargrove@northwestern.edu).

transferred to PC or smartphones for post processing leading to high form factors, high power consumptions or high computing latencies; (2) When multiple sites of sensing are needed, such as muscles from upper arm and forearm, there is a lack of efficient networking schemes to support collaborative classification based on signals from multiple sensing locations; (3) there is a lack of convenient interface to the end users for visual assistance of their operations. To overcome such issues from existing demonstrations, in this paper, we demonstrate a wearable bio-signal processing system using an ultra-low-power system-on-chip (SoC) with a built-in neural network classifier [18]. The features of the proposed system include (1) a single SoC chip with integrated low noise amplifier for EMG/ECG sensing and a built-in neural network classifier with a state-of-art power consumption of only 30μW, which is over a thousand times lower than a commonly used off-the-shelf embedded microprocessor; (2) a collaborative neural network classifier that pre-processes raw channel data from multiple sensing locations and transmits the low dimensional data for final classification leading to a significant saving on data communication, i.e. 50X reduction of inter-site data communication and associated energy; (3) a convenient human interface from a smartphone to provide virtual aids to the user to monitor the classification tasks in real-time. Fig. 1 illustrates the system configuration with the detailed description provided in the following sections.

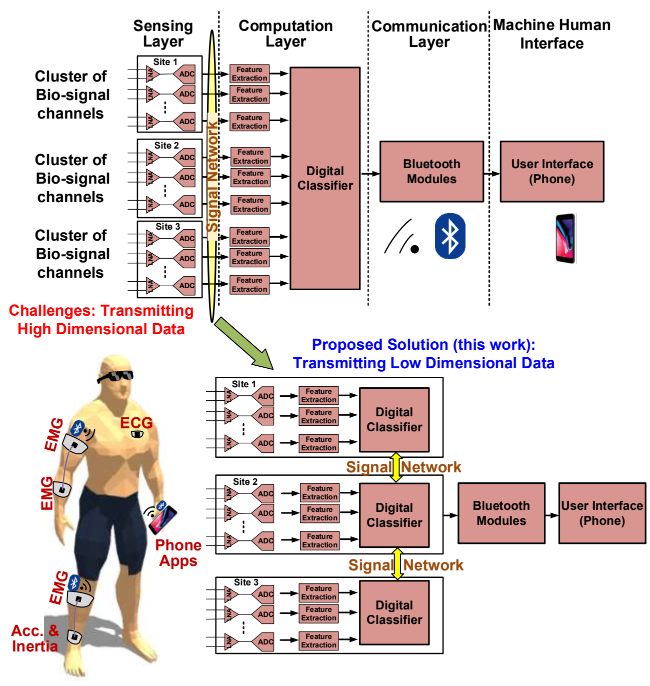


Fig 1: Proposed bio-signal classification system with communication of only low dimensional data from the classifiers.

II. CHALLENGES & METHODS

Fig. 1 shows the overall signal flow of a bio-signal sensing and classification system. A typical system consists of a sensing layer for analog amplification and analog to digital conversion, a computation layer for feature extraction, and classification of bio-signals, a communication layer for data transmission to the external devices, and a human machine interface layer for human interactions. In addition, for real-time operation such as robotic prosthetic arms, a very stringent latency requirement at several millisecond levels is required constraining the time consumed for each layer [19]. The major challenges of such a system are summarized below:

- **Low power consumption for embedded feature extraction and classification:** The power consumption has become the major limiting factor for wearable devices due to the limited battery life. Unfortunately, the digital back-end computation for feature extraction and classification incorporating the modern machine learning algorithms requires a tremendous amount of power. For instance, the widely used TI's OMAP processors in real-time rehabilitation systems consume hundreds of milliwatts of power while another commonly used embedded microprocessor, ST's STM32L151 consumes 35 milliwatts of power [20]. This results in only 10 hours of total operation from a Lithium battery ignoring other system power consumptions, such as analog LNA, ADC, and Bluetooth communications. The high power consumption leads to a constant burden of battery replacement or recharging efforts. To enable sustainable operation of wearable devices, low power operation for digital computation is needed, which requires a special Application Specific Integrated Circuit (ASIC) architectures. In this work, we make use of a customized system-on-chip with fully integrated analog front-end and digital back-end classifier consuming only 30μW power. Different from conventional microprocessors, the design utilizes a neuromorphic architecture which integrates computational neurons for processing neural network leading to ultra-low power consumption and low latency operation, e.g. 5~15ms satisfying the requirement of real-time operation. We especially demonstrated the developed system using an EMG based gesture classification tasks while other signal processing jobs, e.g. ECG or accelerometer based detections, can also be performed from the developed system.

- **Multi-site sensing and collaborative classification:** Based on the locations of sensors or the types of signals being processed, various sites of human body, e.g. arms, legs, are often being sensed simultaneously and the classification tasks commonly require a fusion of all the channels' information. Conventionally, raw data from all the channels at various locations are transmitted into a central location for classification [21]. To achieve such a goal, each site, e.g. upper arm or forearm is provided an analog front-end chip for amplifications and digitalization. The raw digitalized data at each sampling period is transmitted through a network to a centralized location for post-processing. This leads to huge data traffic and energy consumption. As a result, there is a strong benefit of bringing data processing near sensory nodes and only transmitting low dimensional data through the network as demonstrated in this paper. As shown in Fig. 1, we propose an integrated collaborative neural network scheme where the neural network classifier on the SoC chips can collaborate with each other and only low dimensional data is being transmitted over a simple data clock network rendering significant reduction of data traffic. An analysis of the collaborative neural network is provided in this paper.

- **Human Machine Interface for Virtual Aids**: Smartphone has become the most widely used human computing platform. As a result, it is the most convenient method to build a human machine interface between the bio-signal processing system and a smartphone. A wireless communication and visual interface from smartphone Apps bring easy access to the biomedical system for the users or patients. Unfortunately, most of the existing demonstration lacks such a human machine interface. In this work, we developed an Android Apps which works with the bio-signal sensing device and a Bluetooth module to display user-friendly virtual 3D graphs on the smartphone screen. The overall latency of the system is measured to be very short and can be used for many biomedical applications such as online training or diagnosis, augmented reality (AR) assisted rehabilitation and so on.

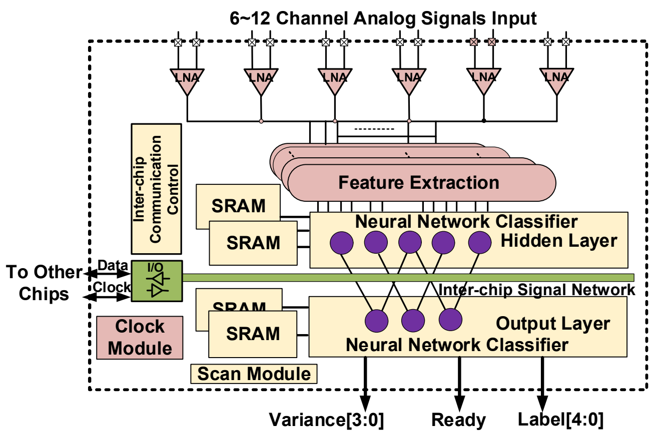


Fig. 2 Ultra-low Power SoC Chip Architecture.

III. Ultra-low-power SoC Architecture

Fig. 2 shows the top-level architecture of the implemented ultra-low-power biomedical signal processing SoC. Up to six channels of differential signals or twelve channels of single-ended channels of analog inputs supporting both wet and dry electrodes are first sent into AC coupled two-stage low noise amplifiers (LNA). A programmable gain of up to 57dB with a bandwidth between 5 Hz to 3 kHz is provided from the LNA suitable for EMG and ECG applications, as well as a variety of other wearable sensors. Mixed-signal circuits at each input channel were implemented to realize analog to digital conversion and feature extractions supporting commonly used time-domain features such as mean, variance, slope sign changes, zero-crossing, and histograms.

A three-layer neural network classifier is implemented for gesture classification from the extracted features. Multiple on-chip SRAM banks with a total size of 5.6kB are used to store the pre-trained 8-bit weights for inference tasks. Different from the conventional microprocessor, the design of the neural network classifier follows a neuromorphic architecture where multiple neurons with integrated multiplier-accumulation (MAC) units and sigmoid activations functions are used to perform the neural network inferences. The use of multiple neurons and separation of neural layers brings an advantage of scalable architecture, i.e. multiple neural networks can collaborate to construct a larger network. As shown in Fig. 2, in multi-chip operation mode, the outputs from intermediate neurons from the hidden layer are transmitted across an inter-chip network through a global bus consisting of data, clock, and a start signal. During networking, each chip is assigned a chip ID with the first chip serving as a master chip and providing a networking clock signal for the rest of the chips. At each clock cycle, every neuron takes turns to transmit its output value bit-by-bit. Once the first chip is finished, the chip with chip ID of 2 will continue until all chips and all neurons finish transmitting. While one chip is transmitting, all the rest chips receive the transmitted data and record the corresponding neuron output by counting the cycles being transmitted. After all communication is finished, the master chip proceeds to finish up the classification of the entire neural network generating resulted labels, as well as a ready signal for triggering external device and optional variance feature values, which are special channel information for subsequent robotic operations when used in prosthetic applications.

IV. Benefits of Low Dimensional Data Transmission

In this section, we perform analysis on the comparison between the conventional data communication scheme and proposed low dimensional data communication scheme as illustrated in Fig. 1. For supporting multiple locations, e.g. gait classification involving upper arm and forearm, or multiple limbs, the physiological signals, e.g. EMG, need to be gathered from multiple sites around the human body. A cluster of multiple channels of EMG signals from the same muscles are sensed at each site. This leads to the requirement of transmitting large amount of multi-bit raw data sampled at each sampling clock period, e.g. kHz, across long distance into a central processing unit for feature extraction and classification in a conventional setting. To realize the data communication, traditionally, analog front-end chip including LNA and ADC is used to sense and digitalize the signals and a data bus, e.g. I2C is used to transfer data across multiple chips [22]. As a result, in a traditional scheme, the total amount of clock cycles (and similarly energy consumption) for transmitting multi-channel data to the central classifier within one classification window can be calculated in equation (1).

$$Cycle_{tot\ \_I2C} = N_{Ch} \times N_{Res} \times f_{sampling} \times t_{window} \qquad (1)$$

where the N_{Ch} is the number of analog signal channels needed to transmit, N_{Res} is the ADC resolution, $f_{sampling}$ is the ADC sampling frequency and the t_{window} is the length for one classification window. Based on equation (1), it is observed that the total amount of clock cycles required for transmission increases proportionally with channel numbers, sampling rate and ADC resolution. As the typical clock frequency of basic I2C protocol is 100 kHz, only 6 channels of data can be transmitted using an 8-bit ADC with 2 kHz sampling rate. Further increase on the number of channels or resolutions will require higher clock frequency with an increase of total energy consumptions. In addition, the volume of data for transmission is significantly large leading to huge communication bottleneck and energy consumption.

Compared with the traditional scheme, in our proposed low dimensional communication (LDC) scheme, instead of transmitting the high dimensional raw signals from each channel, each sensor node performs its own computation of feature extraction and hidden layer neural network computation. The calculated outputs from hidden-layer neurons are transmitted over the communication channel to the rest of the node in the network. Once the transmission is finished, final classification is performed by the master chip to generate the final label. In this communication scheme, the number of clock cycles used and energy costs in one sampling window can be calculated by equation (2).

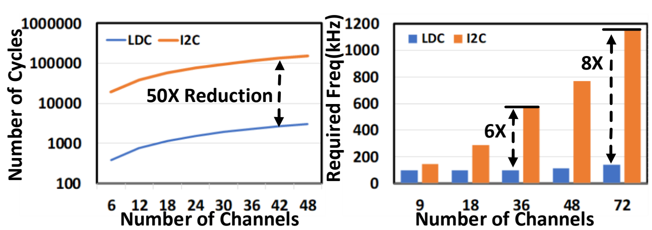
$$Cycle_{total\_LDC} = N_{neuron} \times N_{bit} \times N_{node} \qquad (2)$$

where N_{neuron} is the number of neurons in the hidden layer, N_{bit} is the number of bits of neuron network, N_{node} is the number of chips inside the system.

As an example of our system, 12 channels were used for a two-chip system, the N_{neuron} is 24 in each SoC chip and 8-bit operations are used in the neural network. Assuming the communication clock in the LDC is the same as I2C, $f_{sampling}$ is 2 kHz and t_{window}= 200 ms with 100 ms overlap window in a typical EMG classification application, the saving of data cycles/energy compared to traditional operation can be calculated by equation (3):

$$Ratio_E = Cycle_{total\_I2C}/(2 \times Cycle_{tot\quad LDC})$$

$$= \frac{N_{Ch} \times N_{Res} \times f_{sampling} \times t_{window}}{2 \times N_{neuron} \times N_{bit} \times N_{node}} \qquad (3)$$



(a) (b)

Fig.3 Comparison between the two schemes. (a) Total number of transmission cycles from conventional (I2C) and proposed (LDC) communication schemes with different numbers of channels. (b) Required transmission clock frequency from the two schemes with different numbers of channels.

Fig.3(a) shows the calculation from (3) with various numbers of channels being process. The proposed LDC scheme maintains a 50X saving in total number of cycles compared to the traditional I2C scheme when the number of channels were increased from 6 channels to 48 channels. Fig.3(b) shows the required communication clock frequency in these two communication protocols versus the number of channels in use. In conventional communication scheme, all channels data were directly sent to the classifier. The frequency required to transmit all the data was proportional to the number of channels. In the proposed LDC communication scheme, assuming all channels were evenly divided into three sensor nodes, the required clock frequency only increases from 96kHz to 140kHz with 6 channels to 72 channels leading to 6X to 8X reduction of the required transmission clock frequency. A small increase in the clock frequency was due to the gradual increase of the number of neurons (increased with roughly the square root of the numbers of input channels) to maintain final accuracy when more input channels are connected to each chip. Because the transmission only happens to the pre-processed hidden neurons' output data, the required communication cycles do not increase as fast as the conventional scheme. Minor degradation of classification accuracy is observed from benchmarks of EMG based gesture recognition. The collaborative neural network schemes cause the total classification accuracy rate to drop by around 2% compared with the conventional scheme due to the separation of fully connected neurons.

V. BIO-SIGNAL SYSTEM WITH USER INTERFACE

A bio-signal classification system was built incorporating a bio-signal SoC module, a Bluetooth interface module and a mobile App specially built for Android smartphones.

A. Bio-signal SoC Module

Left of Fig.4(a) shows the implemented bio-signal classification module. This module consists of the bio-signal classification SoC, bias generator circuits, power management chips and digital interface.

The dimension of PCB board is 53 mm x 36 mm, powered by CR2032 coin battery and Texas Instruments TPS745 adjustable LDOs for power management. The TPS 745 LDO provides a wide range of output voltages from 0.55V to 1.8V, suitable for the dynamic voltage frequency scaling (DVFS) operation of the SoC chip as described in Section III whose core voltages can scale from 0.6V to 1.2V. The operation latency requirement must be satisfied when DVFS is applied. Several analog reference voltages were generated on the board by resistor ladders. The outputs of the SoC chip, e.g. classification labels, are directly sent out from the chip to the Bluetooth interface module.

B. Bluetooth Interface Module

Although the SoC module already delivers most of the tasks for real-time classification, to support a convenient human machine interface (HMI), an off-shelf Bluetooth module is utilized for communicating with user's smartphone. Right of the Fig.4(a) shows the Pyboard SF6W module used for Bluetooth communication. The Pyboard SF6W module comes with an STM32F722 microcontroller and a CYW4343 WiFi/ Bluetooth module, which supports programming with micropython language and Bluetooth Low Energy(BLE) communications. SF6W is used in our setup to read output labels from the SoC chip and transmit via BLE protocol to external mobile App.

C. Mobile App for User Interface

An Android mobile App was developed to receive the output labels from the Bluetooth module and emulate virtual arm responses to the output label. The mobile Apps can be used for training of patients with a disability using a prosthetic device. As shown in Fig.4(b), a 3D model of the prosthetic arm is displayed on the mobile App corresponding to the classification results of the bio-signal processing modules with low latency.

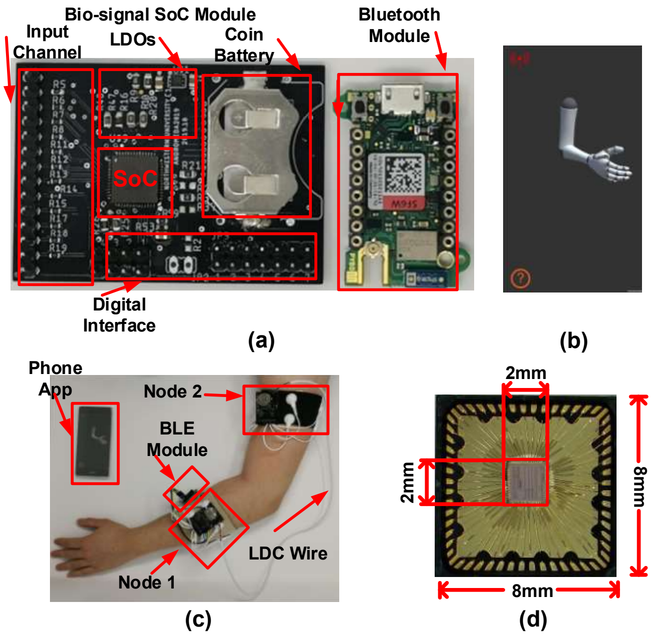


Fig.4 Photos of the developed biomedical system. (a) Bio-signal SoC module with the special SoC, LDO, battery, etc. and Bluetooth module; (b) Screenshot of the mobile App;(c) System setup on a real user; (d) Fabricated chip within a QFN52 package.

VI. RESULTS

The SoC test chip was fabricated in TSMC 65nm low power technology. Fig.4 (d) shows the fabricated chip with a dimension of 2mm by 2mm in a QFN52 package. The total amount of power consumed by the SoC chip is measured at 12 to 30µW with supply voltage between 0.6 to 1.2V when 5-15ms computation latency requirement was fulfilled, which is more than 5X lower than the previous SVM based SoC chip for seizure detection [23] and more than 1100X lower than a conventional embedded solution based on STM32 microprocessor [20]. The supporting LDOs consume 280µW static power, which can be further optimized. Single coin battery can support the SoC module for at least 200 hours.

Fig.4(c) shows the whole system setup on a real user. The measurement procedures were approved by the Northwestern University IRB. Two sensor nodes with an SoC chip at each node were mounted on the upper arm and forearm with a wired communication channel between two nodes. The upper arm node senses the signal from biceps brachii and triceps brachii while the forearm node senses signals from extensor muscles and flexor muscles of the forearm to classify the gestures. The Bluetooth module was connected to the forearm node to read the final output labels from the SoC module and send the labels to the smartphone App. The smartphone App displays the corresponding 3D gesture movement based on the received label.

Fig.5 shows the measured communication waveforms during the gesture classification process. In each half of the 200ms operational window, i.e. 100ms overlapped sampling window, each sensor node samples multiple channels' EMG signals. The rising/falling edge of the global start signal triggers each sensor node to propagate their features into the hidden layer of neural network classifier for processing, requiring about 1ms to complete. Each node subsequently sends out their hidden layer neuron output data, with around 4ms delay per node. Once all networking neurons finish data transmission, the output layer of the neural network in the master chip will complete the inference tasks and send out the label and ready signal to the Bluetooth module. The total processing time for two nodes was measured at around 10ms as in Fig. 5. The following 6 spikes of the ready signal are the variance values of a selected channel for the use of external prosthetic devices.

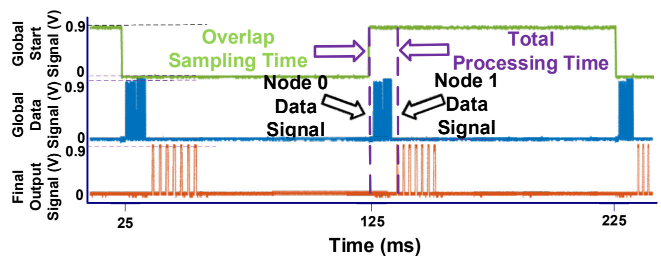


Fig. 5 Measured waveforms of operations of two-chip system.

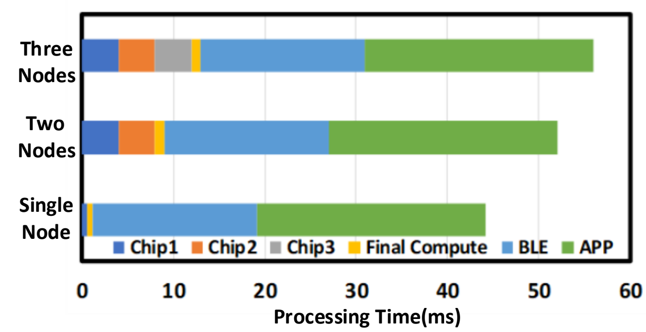


Fig. 6 Measured processing time breakdown in single node, two nodes and three nodes operation.

Fig.6 shows the measured latency breakdown in a single node, two nodes, and three nodes operation modes. The time was measured by the rising edge of the start signal to the time the App starts to respond to the classification label. In the single node's operation mode, the fastest response of 1.2ms was observed since the neural network proceeded without waiting for any data from the other nodes. In multi-node operations, each chip takes about 4ms to broadcast their data and the master chip takes 1ms to complete the operation with a total of 9ms and 13ms processing time in two nodes and three nodes setting respectively. The total operation time was dominated by the Bluetooth module's transmission time and mobile app's response time. The BLE module has an 18ms delay based on measurement. The smartphone App has a 25ms response time from the operating system. The total latency of the whole system is about 60ms, which is fast enough for any direct user interface operation. Note that in a real-time system such as a robotic prosthetic arm where latency is critical, the SoC chip supports the required latency of only a few milliseconds. The BLE and Apps are only for user interface and do not require extremely fast response.

VII. CONCLUSION

In this paper, we present a wearable bio-signal classification device for real-time applications. The system includes a specially designed ultra-low power SoC, a Bluetooth interface module and a smartphone App for low latency applications such as prosthetics for rehabilitations. The SoC only consumes 30µW and embeds a collaborative neural network classifier which allows only low dimensional data being transmitted across multiple chips for multi-site classification. A demonstration of EMG based gesture classification showed more than 1100X power reduction from the SoC chip compared with the conventional embedded solution. A 50X reduction in data communication with low latency in real-time operation was also achieved due to the collaborative neural network classifier from the developed system.

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